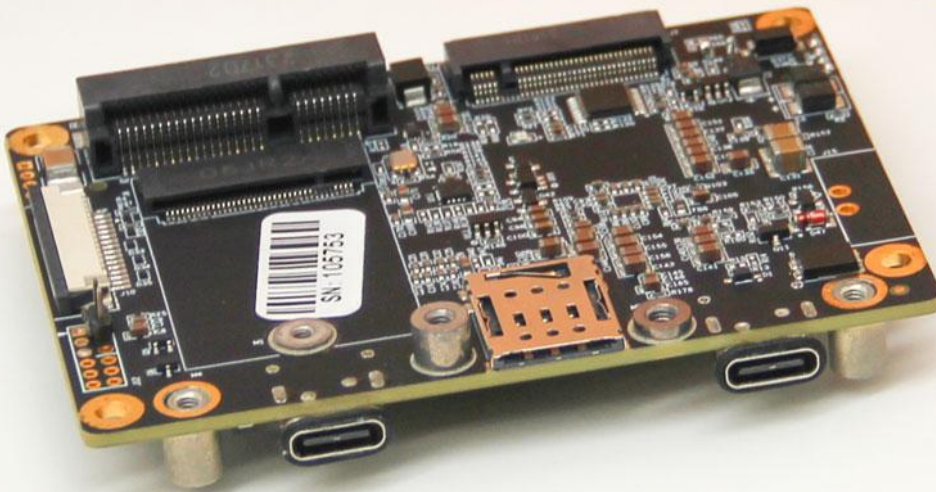




AI Development Carrier Board

Y-C17

Datasheet



Version V2.1

Date 2025-01-08

Copyright by Beijing Plink-AI Technology Co., LTD.2023.All rights reserved.

No part of this document may be reproduced or transmitted in any form or by any means without prior written consent of Plink-AI Technologies Co., Ltd.

Notice

The purchased products, services and features are stipulated by the contract made between Plink-AI and the customer. All or part of the products, services and features described in this document may not be within the purchase scope or the usage scope. Unless otherwise specified in the contract, all statements, information, and recommendations in this document are provided "AS IS" without warranties, guarantees or representations of any kind, either express or implied.

The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied.

Please scan code for more products



Website



WeChat Channel

Beijing Plink-AI Technology Co., LTD

Web: <http://www.plink-ai.com/>

Add: Room 1106/1108, Jinyu Jiahua Building, Shangdi 3rd Street, Haidian District,
Beijing

Tel: +86-010-62962285/400-127-3302

Document History

Version	Date	Description of Change	Hardware Version
V 1.0	2023-4-21	Preliminary Release	V 1.0
V 2.0	2024-1-9	Modify the product manual template; Added interface test description; Added Jetpack5.* version GPIO mapping number;	V 1.0
V 2.0	2025-1-8	Modify font	V 1.0

Hardware Update History

Version	Date	Description of Change
V 1.0	2023-4-21	Initial version



Electronic components and circuits are very sensitive to electrostatic discharge, although the company will design the main interface on the board card to do anti-static protection design, but it is difficult to do anti-static safety protection for all components and circuits. Therefore, it is recommended that you take ESD safety measures when handling any circuit board component.

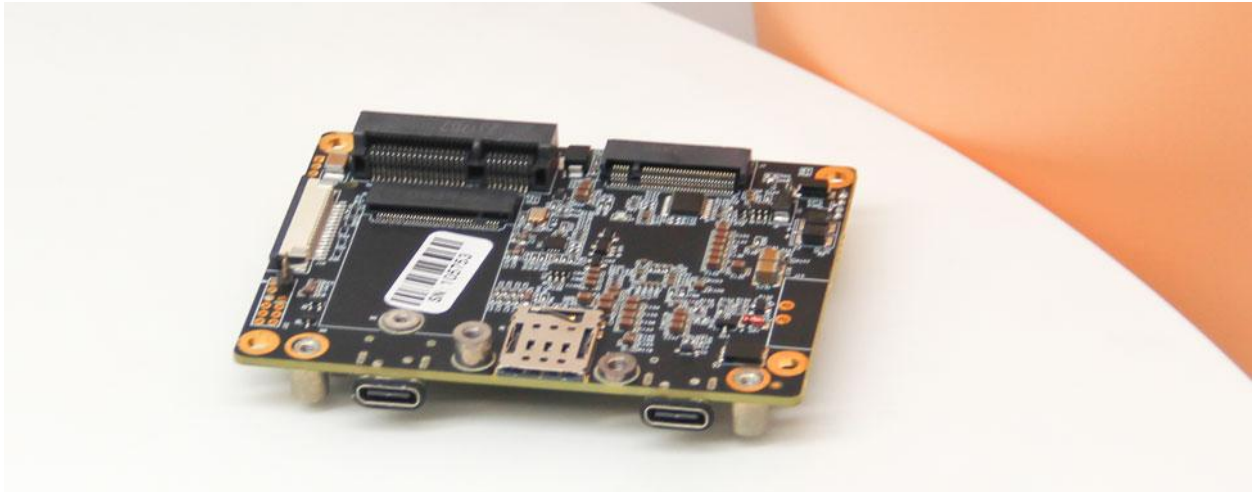
ESD safety measures include but are not limited to the following:

1. Put the card in an ESD bag during transportation or storage. Do not take out the card until installation and deployment.
2. Before touching the board, release the static electricity stored in the body: Wear a grounding wrist strap.
3. Operate circuit boards only in electrostatic discharge safe areas.
4. Avoid moving circuit boards in carpeted areas.
5. Avoid direct contact with electronic components on the board through edge contact.

Table of Contents

1 Introduction-----	6
2 Specifications-----	7
3 External I/O Ports-----	10
4 All-Round Display-----	12
5 Connector Description-----	13
6 Ordering Information-----	24
7 Recovery Mode-----	24
8 Method of Application-----	25
9 GPIO Test-----	26
10 Serial Port Test-----	27
11 Special Instructions-----	28
12 Signal Separation Board-----	29

1 Introduction



Y-C17 is an interface board equipped with NVIDIA Jetson Orin NX/Orin Nano/Xavier NX series core modules. The whole board device adopts wide temperature industrial model, the main interface is designed for electrostatic safety protection, and the power supply application scheme with high reliability is adopted. The input power supply has the function of overvoltage and reverse polarity protection. With a rich external interface, it can be equipped with hundreds of functional modules through a miniPCIe connector (including USB2.0 and PCIe X1 signals) to achieve further expansion of system functions.

The Y-C17 power input interface is not welded by default, so it should be used with a signal separation board. When using, please follow the screen printing on the signal separation board and correctly connect the positive and negative electrodes of the power cord. After the power cable is connected, please follow the signal separation board installation example and connect it to Y-C17 before powering the carrier board. **If the signal separation board is not used, please solder the power supply input interface by yourself, and do not connect any equipment to the J2 interface of Y-C17. The J2 interface does not support standard USB functionality. Accessing the device is easy to cause the device to burn.**

2 Specifications

	Specific
Carrier Board	Y-C17
Module	NVIDIA Jetson Orin NX/Orin Nano/Xavier NX Series Modules
Temperature	-40 ~ +85°C
Dimensions (L×W×H)	85mm * 63mm * 18mm (Including I/O ports and mounting holes)
Weight	45g

Power Supply	Spec
Input Type	DC
Input Voltage	+12V ~ +24V

I/O Ports

Interface	Quantity	Interface	Quantity
Type-C	2	Nano SIM Card Slot	1
miniPCle Slot	1	2 Lane MIPI CSI	1
M.2 Key M Slot (2230)	1	M.2 Key B Slot(3050)	1
RTC Battery Connector	1	Fan Header(5V)	1
Multi	1*i2c/4*GPIO/1*PSDK(uart + usb)		

NVIDIA Jetson Series Modules

Technical Specifications

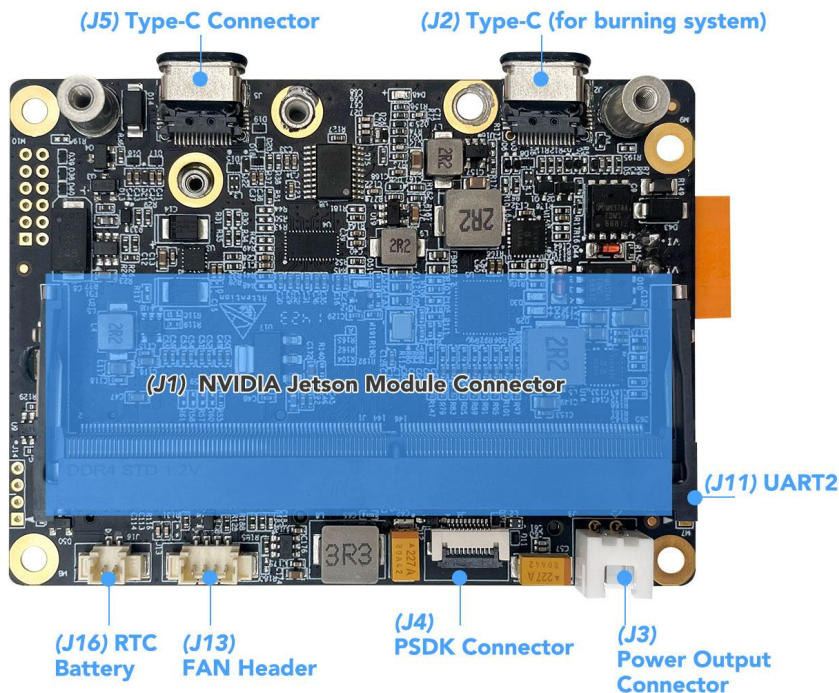
Module	Jetson ORIN NX 16GB	Jetson ORIN NX 8GB	Jetson Orin Nano 8GB	Jetson Orin Nano 4GB
AI Performance	100 TOPS	70 TOPS	40 TOPS	20 TOPS
GPU	1024-core NVIDIA Ampere architecture GPU with 32 Tensor Cores		1024-core NVIDIA Ampere architecture GPU with 32 Tensor Cores	512-core NVIDIA Ampere architecture GPU with 16 Tensor Cores
CPU	8-core Arm® Cortex®-A78AE v8.2 64-bit CPU 2MB L2 + 4MB L3	6-core Arm® Cortex®-A78AE v8.2 64-bit CPU 1.5MB L2 + 4MB L3	6-core Arm® Cortex®-A78AE v8.2 64-bit CPU 1.5MB L2 + 4MB L3	
Memory	16GB 128-bit LPDDR5 102.4GB/s	8GB 128-bit LPDDR5 102.4GB/s	8GB 128-bit LPDDR5 68 GB/s	4GB 64-bit LPDDR5 34 GB/s
Storage	Support external NVME		Support external NVME	
Video Encode	1x 4K60 (H.265) 3x 4K30 (H.265) 6x 1080p60 (H.265) 12x 1080p30 (H.265)		1080p30 supported by 1-2 CPU cores	
Video Decode	1x 8K30 (H.265) 2x 4K60 (H.265) 4x 4K30 (H.265) 9x 1080p60 (H.265) 18x 1080p30 (H.265)		1x 4K60 (H.265) 2x 4K30 (H.265) 5x 1080p60 (H.265) 11x 1080p30 (H.265)	
Power	10W - 25W	10W - 20W	7W - 15W	7W - 10W

NVIDIA Jetson Series Modules

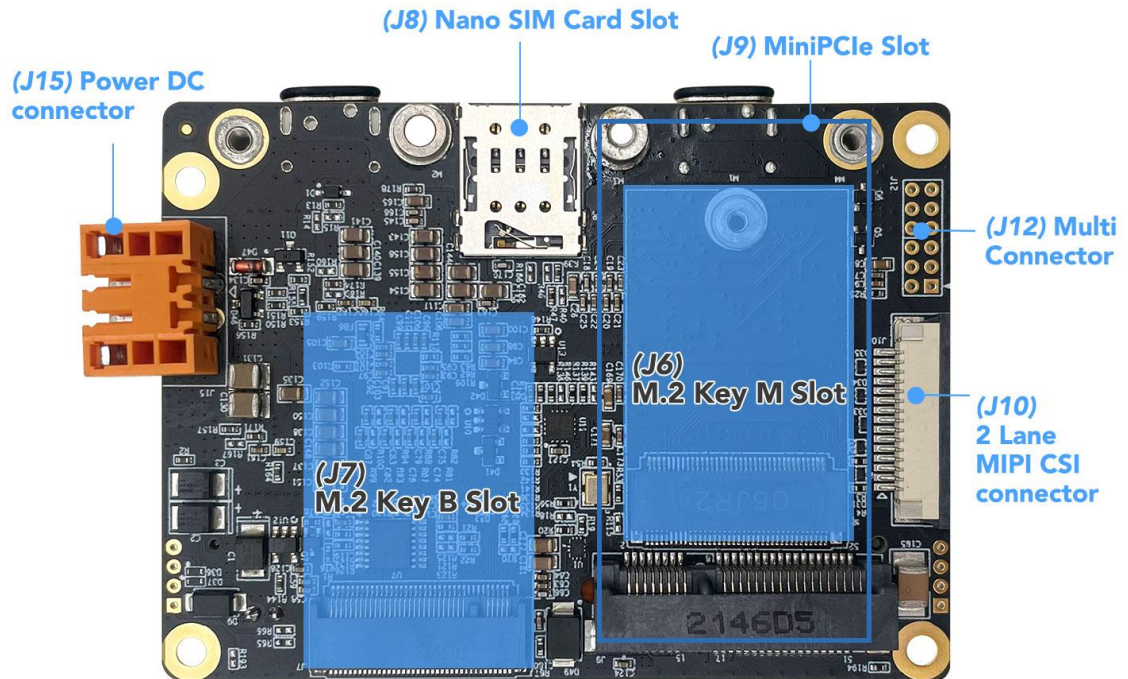
Technical Specifications

Module	Xavier NX 16GB	Xavier NX 8GB
AI Performance	21TOPS	
GPU	384-core NVIDIA Volta™ architecture GPU with 48 Tensor Cores	
CPU	6-core NVIDIA Carmel Arm®v8.2 64-bit CPU 6MB L2 + 4MB L3	
Memory	16 128-bit LPDDR4x 59.7GB/s	8GB 128-bit LPDDR4x 59.7GB/s
Storage	16GB eMMC 5.1	
Video Encode	2x 4K60 (H.265) 4x 4K30 (H.265) 10x 1080p60 (H.265) 22x 1080p30 (H.265)	
Video Decode	2x 8K30 (H.265) 6x 4K60 (H.265) 12x 4K30 (H.265) 22x 1080p60 (H.265) 44x 1080p30 (H.265)	
Power	10W – 20W	
Mechanical	69.6mm x 45mm 260-pin SO-DIMM connector	

3 External I/O Ports



Sign	Function	Sign	Function
J1	Jetson Module Connector	J3	Power Output Connector
J13	Fan Header	J11	UART2 (Debug)
J16	RTC Battery Connector	J5	Standard USB Type C
J4	PSDK Signal Interface	J2	Type C Connector (Check the connector description in detail)

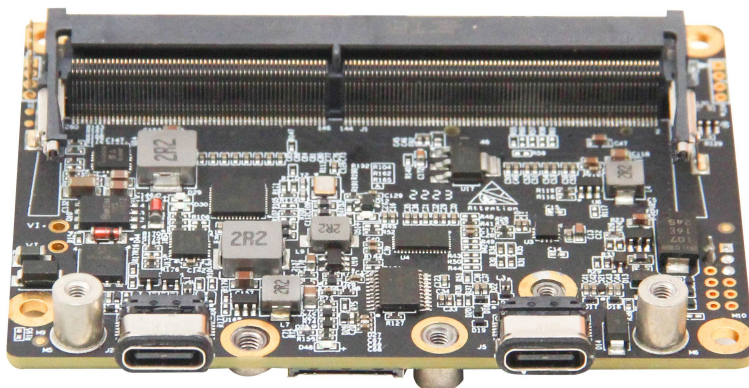


Sign	Function	Sign	Function
J6	M.2 Key M Slot(2230)	J9	miniPCle Slot
J7	M.2 Key B Slot(3050)	J10	2 Lane MIPI CSI Connector
J8	Nano Sim Card Slot	J15	Power Jack (Actual unwelded)
J12	Multi Connector(4 * GPIO / 1 * i2c)		

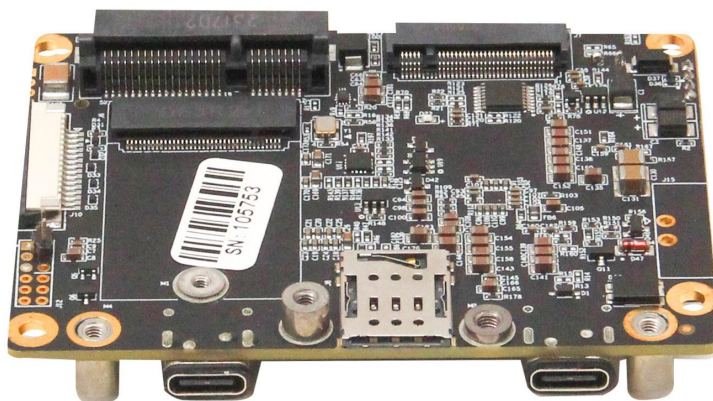
LED

Sign	Function
D51	Core module operating status indicator
D48	Carrier power supply status indicator

4 All-Round Display

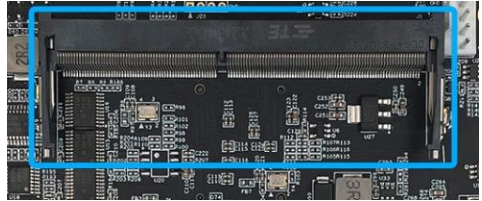


Front

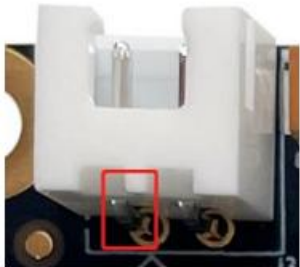


Back

5 Connector Description

Jetson Module Connector (J1)		
Function	Connect NVIDIA Jetson Orin NX / Orin Nano/Xavier NX series modules	
Sign	J1	
Type/Model	2309413-1	
Explain	For pin definitions of this connector, refer to the pin definition instructions in the NVIDIA Jetson Series Orin NX Core Module data book	

Power Output Interface (J3)				
Function	The output voltage is 0.3V lower than the input voltage.			
Sign	J3			
Type/Model	XH-2AW			
Pin definition	Pin	Signal	Pin	Signal
	1	VOUT	2	GND
Pin 1 position: right picture identification.				



Type -C Connector (J2)

Function	Type C Connector, Use to flash system or connect to a DJI drone			
Sign	J2			
Type/Model	Standard Type C male connector			
Pin definition	Pin	Signal	Pin	Signal
	A1	GND	B1	GND
	A2	NC	B2	GPIO13_PWM_3V3
	A3	FORCE_RECOVERY	B3	NC
	A4	SVIN	B4	SVIN
	A5	GPIO06_PPS_3V3	B5	UART0_TX_3V3
	A6	GPIO07_SELECT	B6	USB0_P
	A7	USB0_VBUS_EN0	B7	USB0_N
	A8	GND	B8	UART0_RX_3V3
	A9	SVIN	B9	SVIN
	A10	NC	B10	NC
	A11	NC	B11	NC
	A12	GND	B12	GND
	This interface does not support USB function, can be used for system power input, with the company's self-developed signal separation board used, mainly used for system burning. It can be used to connect DJI drones. For more details, please consult our technical staff.			



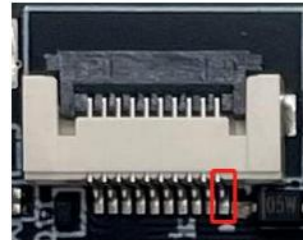


Type -C Connector (J5)

Function	USB3.0 Type C Connector																																																								
Sign	J5																																																								
Type/Model	Standard Type C male connector																																																								
Pin definition	<table><thead><tr><th>Pin</th><th>Signal</th><th>Pin</th><th>Signal</th></tr></thead><tbody><tr><td>A1</td><td>GND</td><td>B1</td><td>GND</td></tr><tr><td>A2</td><td>TX1_P</td><td>B2</td><td>TX2_P</td></tr><tr><td>A3</td><td>TX1_N</td><td>B3</td><td>TX2_N</td></tr><tr><td>A4</td><td>VBUS</td><td>B4</td><td>VBUS</td></tr><tr><td>A5</td><td>CC1</td><td>B5</td><td>CC2</td></tr><tr><td>A6</td><td>USB1_P</td><td>B6</td><td>USB1_P</td></tr><tr><td>A7</td><td>USB1_N</td><td>B7</td><td>USB1_N</td></tr><tr><td>A8</td><td>SBU1</td><td>B8</td><td>SBU2</td></tr><tr><td>A9</td><td>VBUS</td><td>B9</td><td>VBUS</td></tr><tr><td>A10</td><td>RX2_N</td><td>B10</td><td>RX1_N</td></tr><tr><td>A11</td><td>RX2_P</td><td>B11</td><td>RX1_P</td></tr><tr><td>A12</td><td>GND</td><td>B12</td><td>GND</td></tr></tbody></table>	Pin	Signal	Pin		Signal	A1	GND	B1	GND	A2	TX1_P	B2	TX2_P	A3	TX1_N	B3	TX2_N	A4	VBUS	B4	VBUS	A5	CC1	B5	CC2	A6	USB1_P	B6	USB1_P	A7	USB1_N	B7	USB1_N	A8	SBU1	B8	SBU2	A9	VBUS	B9	VBUS	A10	RX2_N	B10	RX1_N	A11	RX2_P	B11	RX1_P	A12	GND	B12	GND	This interface is a standard USB Type C interface, and the display of the Y-C17 carrier board needs to be external to the USB Type C hub output supporting HDMI display through this interface.		
	Pin	Signal	Pin	Signal																																																					
	A1	GND	B1	GND																																																					
	A2	TX1_P	B2	TX2_P																																																					
	A3	TX1_N	B3	TX2_N																																																					
	A4	VBUS	B4	VBUS																																																					
	A5	CC1	B5	CC2																																																					
	A6	USB1_P	B6	USB1_P																																																					
	A7	USB1_N	B7	USB1_N																																																					
	A8	SBU1	B8	SBU2																																																					
	A9	VBUS	B9	VBUS																																																					
	A10	RX2_N	B10	RX1_N																																																					
	A11	RX2_P	B11	RX1_P																																																					
A12	GND	B12	GND																																																						

PSDK Signal Interface (J4)

Function	The PSDK connector is used to connect the usb2.0+uart of the DJI UAV extension			
Sign	J4			
Type/Model	FPC_0R5MM_10P			
Pin definition	Pin	Signal	Pin	Signal
	1	5V	2	GND
	3	GND	4	GND
	5	UART1_TX_3V3	6	UART1_RX_3V3
	7	GND	8	USB2_D1_N
	9	USB2_D1_P	10	GND
	Pin 1 position: right picture identification.			

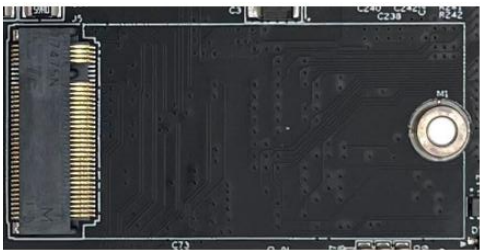


Fan Header (J13)

Function	4-pin fan header for 12V PWM fan			
Sign	J13			
Type/Model	Molex PicoBlade Header 53261-0471			
Pin definition	Pin	Signal	Pin	Signal
	1	GND	2	POWER (+5V)
	3	TACH	4	PWM
Pin 1 position: right picture identification.				



M.2 Key M Slot (J6)

Function	M.2 Key M Slot	
Sign	J6	
Type/Model	M Key , 2230 Size	

Pin definition

引脚	信号	引脚	信号	引脚	信号
1	GND	2	VCC_3V3	3	GND
4	VCC_3V3	5	PCIE0_RX3_N	6	NC
7	PCIE0_RX3_P	8	NC	9	GND
10	NC	11	PCIE0_TX3_N	12	VCC_3V3
13	PCIE0_TX3_P	14	VCC_3V3	15	GND
16	VCC_3V3	17	PCIE0_RX2_N	18	VCC_3V3
19	PCIE0_RX2_P	20	NC	21	GND
22	NC	23	PCIE0_TX2_N	24	NC
25	PCIE0_TX2_P	26	NC	27	GND
28	NC	29	PCIE0_RX1_N	30	NC
31	PCIE0_RX1_P	32	NC	33	GND
34	NC	35	PCIE0_TX1_N	36	NC
37	PCIE0_TX1_P	38	NC	39	GND
40	I2C2_SCL_1V8	41	PCIE0_RX0_N	42	I2C2_SDA_1V8
43	PCIE0_RX0_P	44	M2_KEYM_ALERT_N_1V8	45	GND
46	NC	47	PCIE0_TX0_N	48	NC
49	PCIE0_TX0_P	50	PCIE0_RST_N_3V3	51	GND
52	PCIE0_CLKREQ_N_3V3	53	PCIE0_CLK_P	54	PCIE_WAKE_N_3V3
55	PCIE0_CLK_N	56	NC	57	GND
58	NC	59	NC	60	NC
61	NC	62	NC	63	NC
64	NC	65	NC	66	NC
67	NC	68	SUSCLK(32KHz)	69	NC
70	VCC_3V3	71	GND	72	VCC_3V3
73	GND	74	VCC_3V3	75	GND

M.2 Key B Slot (J7)

Function	M.2 Key B Slot																																																																																																																																																													
Sign	J7																																																																																																																																																													
Type/Model	B Key , 3050 Size																																																																																																																																																													
Pin definition	<table><tr><th>Pin</th><th>Signal</th><th>Pin</th><th>Signal</th><th>Pin</th><th>Signal</th></tr><tr><td>1</td><td>NC</td><td>2</td><td>VCC_3V8</td><td>3</td><td>GND</td></tr><tr><td>4</td><td>VCC_3V8</td><td>5</td><td>GND</td><td>6</td><td>VCC_1V8</td></tr><tr><td>7</td><td>NC</td><td>8</td><td>VCC_1V8</td><td>9</td><td>NC</td></tr><tr><td>10</td><td>RM_WWAN_LED_N</td><td>11</td><td>GND</td><td>12</td><td>NC</td></tr><tr><td>13</td><td>NC</td><td>14</td><td>NC</td><td>15</td><td>NC</td></tr><tr><td>16</td><td>NC</td><td>17</td><td>NC</td><td>18</td><td>NC</td></tr><tr><td>19</td><td>NC</td><td>20</td><td>NC</td><td>21</td><td>NC</td></tr><tr><td>22</td><td>NC</td><td>23</td><td>VCC_1V8</td><td>24</td><td>NC</td></tr><tr><td>25</td><td>NC</td><td>26</td><td>RM_B_CORE_OUT_1V8</td><td>27</td><td>GND</td></tr><tr><td>28</td><td>NC</td><td>29</td><td>NC</td><td>30</td><td>RM_USIM_RESET</td></tr><tr><td>31</td><td>NC</td><td>32</td><td>RM_USIN_CLK</td><td>33</td><td>GND</td></tr><tr><td>34</td><td>RM_USIM_DATA</td><td>35</td><td>NC</td><td>36</td><td>RM_USIM_PWR</td></tr><tr><td>37</td><td>NC</td><td>38</td><td>VCC_1V8</td><td>39</td><td>GND</td></tr><tr><td>40</td><td>NC</td><td>41</td><td>RM_PCIE_TX_N</td><td>42</td><td>NC</td></tr><tr><td>43</td><td>RM_PCIE_TX_P</td><td>44</td><td>NC</td><td>45</td><td>GND</td></tr><tr><td>46</td><td>NC</td><td>47</td><td>RM_PCIE_RX_N</td><td>48</td><td>NC</td></tr><tr><td>49</td><td>RM_PCIE_RX_P</td><td>50</td><td>RM_RST_N_3V3</td><td>51</td><td>GND</td></tr><tr><td>52</td><td>RM_PCIE_CLK_N_3V3</td><td>53</td><td>RM_PCIE_REFCLK_N</td><td>54</td><td>RM_PCIE_WAKE_N_3V3</td></tr><tr><td>55</td><td>RM_PCIE_REFCLK_P</td><td>56</td><td>NC</td><td>57</td><td>GND</td></tr><tr><td>58</td><td>NC</td><td>59</td><td>NC</td><td>60</td><td>NC</td></tr><tr><td>61</td><td>NC</td><td>62</td><td>NC</td><td>63</td><td>NC</td></tr><tr><td>64</td><td>NC</td><td>65</td><td>NC</td><td>66</td><td>RM_USIM_DET</td></tr><tr><td>67</td><td>RM_RESET_N</td><td>68</td><td>VCC_1V8</td><td>69</td><td>NC</td></tr><tr><td>70</td><td>VCC_3V8</td><td>71</td><td>GND</td><td>72</td><td>VCC_3V8</td></tr><tr><td>73</td><td>GND</td><td>74</td><td>VCC_3V8</td><td>75</td><td>NC</td></tr></table>	Pin	Signal	Pin	Signal	Pin	Signal	1	NC	2	VCC_3V8	3	GND	4	VCC_3V8	5	GND	6	VCC_1V8	7	NC	8	VCC_1V8	9	NC	10	RM_WWAN_LED_N	11	GND	12	NC	13	NC	14	NC	15	NC	16	NC	17	NC	18	NC	19	NC	20	NC	21	NC	22	NC	23	VCC_1V8	24	NC	25	NC	26	RM_B_CORE_OUT_1V8	27	GND	28	NC	29	NC	30	RM_USIM_RESET	31	NC	32	RM_USIN_CLK	33	GND	34	RM_USIM_DATA	35	NC	36	RM_USIM_PWR	37	NC	38	VCC_1V8	39	GND	40	NC	41	RM_PCIE_TX_N	42	NC	43	RM_PCIE_TX_P	44	NC	45	GND	46	NC	47	RM_PCIE_RX_N	48	NC	49	RM_PCIE_RX_P	50	RM_RST_N_3V3	51	GND	52	RM_PCIE_CLK_N_3V3	53	RM_PCIE_REFCLK_N	54	RM_PCIE_WAKE_N_3V3	55	RM_PCIE_REFCLK_P	56	NC	57	GND	58	NC	59	NC	60	NC	61	NC	62	NC	63	NC	64	NC	65	NC	66	RM_USIM_DET	67	RM_RESET_N	68	VCC_1V8	69	NC	70	VCC_3V8	71	GND	72	VCC_3V8	73	GND	74	VCC_3V8	75	NC	
	Pin	Signal	Pin	Signal	Pin	Signal																																																																																																																																																								
	1	NC	2	VCC_3V8	3	GND																																																																																																																																																								
	4	VCC_3V8	5	GND	6	VCC_1V8																																																																																																																																																								
	7	NC	8	VCC_1V8	9	NC																																																																																																																																																								
	10	RM_WWAN_LED_N	11	GND	12	NC																																																																																																																																																								
	13	NC	14	NC	15	NC																																																																																																																																																								
	16	NC	17	NC	18	NC																																																																																																																																																								
	19	NC	20	NC	21	NC																																																																																																																																																								
	22	NC	23	VCC_1V8	24	NC																																																																																																																																																								
	25	NC	26	RM_B_CORE_OUT_1V8	27	GND																																																																																																																																																								
	28	NC	29	NC	30	RM_USIM_RESET																																																																																																																																																								
	31	NC	32	RM_USIN_CLK	33	GND																																																																																																																																																								
	34	RM_USIM_DATA	35	NC	36	RM_USIM_PWR																																																																																																																																																								
	37	NC	38	VCC_1V8	39	GND																																																																																																																																																								
	40	NC	41	RM_PCIE_TX_N	42	NC																																																																																																																																																								
	43	RM_PCIE_TX_P	44	NC	45	GND																																																																																																																																																								
	46	NC	47	RM_PCIE_RX_N	48	NC																																																																																																																																																								
	49	RM_PCIE_RX_P	50	RM_RST_N_3V3	51	GND																																																																																																																																																								
	52	RM_PCIE_CLK_N_3V3	53	RM_PCIE_REFCLK_N	54	RM_PCIE_WAKE_N_3V3																																																																																																																																																								
	55	RM_PCIE_REFCLK_P	56	NC	57	GND																																																																																																																																																								
	58	NC	59	NC	60	NC																																																																																																																																																								
	61	NC	62	NC	63	NC																																																																																																																																																								
	64	NC	65	NC	66	RM_USIM_DET																																																																																																																																																								
	67	RM_RESET_N	68	VCC_1V8	69	NC																																																																																																																																																								
	70	VCC_3V8	71	GND	72	VCC_3V8																																																																																																																																																								
	73	GND	74	VCC_3V8	75	NC																																																																																																																																																								

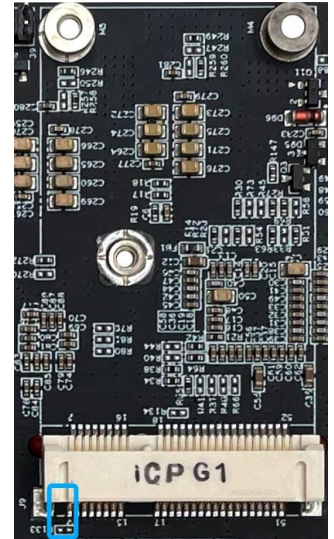
RTC Battery Socket (J16)

Function	Provides power support for the core board clock circuit											
Sign	J16											
Type/Model	Molex PicoBlade Header 53398-0271											
Pin definition	<table><tr><th>Pin</th><th>Signal</th><th>Pin</th><th>Signal</th></tr><tr><td>1</td><td>VCC (3.3V)</td><td>2</td><td>GND</td></tr></table> Pin 1 position: right picture identification.					Pin	Signal	Pin	Signal	1	VCC (3.3V)	2
Pin	Signal	Pin	Signal									
1	VCC (3.3V)	2	GND									

SIM Card Slot (J8)

Function	Nano SIM Card Slot			
Sign	J8			
Type/Model	Nano SIM Card Slot			
Pin definition	Pin	Signal	Pin	Signal
	C1	USIM_PWR	C2	USIM_RESET
	C3	USIM_CLK	C5	GND
	C6	NC	C7	USIM_DATA
	CD	USIM_DET		

miniPCle Slot (J9)				
Function	miniPCle Slot			
Sign	J9			
Type/Model	5.6mm high, support full-length expansion cards.			
Pin definition	Pin	Signal	Pin	Signal
	1	PCIE_WAKE_N	2	VCC_3V3_PCIE
	3	NC	4	GND
	5	NC	6	VCC_1V5_PCIE
	7	PEIC1_CLKREQ_N	8	NC
	9	GND	10	NC
	11	PEIC1_CLK_N	12	NC
	13	PEIC1_CLK_P	14	NC
	15	GND	16	NC
	17	NC	18	GND
	19	NC	20	NC
	21	GND	22	PEIC1_RST_N_3V3
	23	PCIE1_RX0_N	24	VCC_3V3_PCIE
	25	PCIE1_RX0_P	26	GND
	27	GND	28	VCC_1V5_PCIE
	29	GND	30	NC
	31	PCIE1_TX0_N	32	NC
	33	PCIE1_TX0_P	34	GND
	35	GND	36	USB2_D2_N
	37	GND	38	USB2_D2_P
	39	VCC_3V3_PCIE	40	GND
	41	VCC_3V3_PCIE	42	NC
	43	GND	44	NC
	45	NC	46	NC
	47	NC	48	VCC_1V5_PCIE
	49	NC	50	GND
	51	NC	52	VCC_3V3_PCIE



Power Jack (J15)				
Function	Power supply input terminal			
Sign	J15			
Type/Model	No welding by default			
Pin definition	Pin	Signal	Pin	Signal
	1	VCC (+)	2	GND (-)
	Pin 1 position: right picture identification. Input voltage range: +12V~+24V			



Debug Serial Port UART2 (J11)				
Function	Debug Serial Port UART2			
Sign	J11			
Type/Model	2.00 mm pitch, 1*4pin(No welding by default)			
Pin definition	Pin	Signal	Pin	Signal
	1	1V8	2	UART2_TX_1V8
	3	UART2_RX_1V8	4	GND
UART2 defaults to the kernel debugging serial port, which is used to output C-BOOT, U-BOOT and Linux kernel information. After the Linux kernel is started, it is used as the serial port of the display and control terminal, and the default serial port is set to: 115200, 8N1 .				



MIPI CSI (J10)

Function 2 Lane MIPI CSI Camera Connector

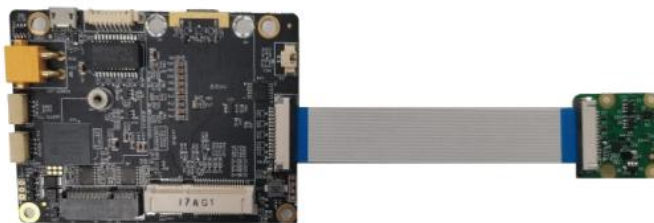
Sign J10

Type/Model 15pin, 1.0mm pitch, Lower contact FPC connector

Pin definition

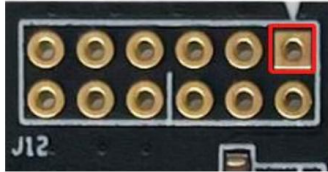
Pin	Signal	Pin	Signal
1	VCC_3V3	2	CAM_I2C_SDA_3V3
3	CSI1_D0_P	4	CAM0_MCLK_1V8
5	CAM0_PWDN_1V8	6	GND
7	CSI0_CLK_P	8	CSI0_CLK_N
9	GND	10	CSI0_D1_P
11	CSI0_D1_N	12	GND
13	CSI0_D0_P	14	CSI0_D0_N
15	GND		

Connection diagram with the Raspberry PI Generation 2 MIPI camera, note the need to use the same plane cable link.



Pin 1 position: right picture identification.



12-pin Expansion Header (J12)																																
Function	Multi-function signal extension interface																															
Sign	J12																															
Type/Model	2.0mm pitch, 2*6pin																															
Pin definition	<table><tr><th>Pin</th><th>Signal</th><th>Pin</th><th>Signal</th></tr><tr><td>1</td><td>VCC_5V</td><td>2</td><td>VCC_3V3</td></tr><tr><td>3</td><td>GND</td><td>4</td><td>GND</td></tr><tr><td>5</td><td>GPIO01</td><td>6</td><td>GPIO03</td></tr><tr><td>7</td><td>GPIO02</td><td>8</td><td>GPIO04</td></tr><tr><td>9</td><td>GND</td><td>10</td><td>GND</td></tr><tr><td>11</td><td>I2C1_SCL_3V3</td><td>12</td><td>I2C1_SDA_3V3</td></tr></table>	Pin	Signal	Pin	Signal	1	VCC_5V	2	VCC_3V3	3	GND	4	GND	5	GPIO01	6	GPIO03	7	GPIO02	8	GPIO04	9	GND	10	GND	11	I2C1_SCL_3V3	12	I2C1_SDA_3V3			
	Pin	Signal	Pin	Signal																												
	1	VCC_5V	2	VCC_3V3																												
	3	GND	4	GND																												
	5	GPIO01	6	GPIO03																												
	7	GPIO02	8	GPIO04																												
	9	GND	10	GND																												
	11	I2C1_SCL_3V3	12	I2C1_SDA_3V3																												
	I2C device file names mapped in the system are shown in the following table:																															
	<table><tr><th>Xavier NX</th><th>ORIN NX</th><th>ORIN NANO</th></tr><tr><td>/dev/i2c-8</td><td>/dev/i2c-7</td><td>/dev/i2c-7</td></tr></table>	Xavier NX	ORIN NX	ORIN NANO	/dev/i2c-8	/dev/i2c-7	/dev/i2c-7																									
Xavier NX	ORIN NX	ORIN NANO																														
/dev/i2c-8	/dev/i2c-7	/dev/i2c-7																														
The resulting GPIO mapping numbers are shown in the following table. GPIO high level voltage is 3.3V.																																
<table><tr><th></th><th>GPIO01</th><th>GPIO02</th><th>GPIO03</th><th>GPIO04</th></tr><tr><td>Xavier NX(<=L4T32.*)</td><td>421</td><td>419</td><td>264</td><td>265</td></tr><tr><td>Xavier NX(>L4T 32.*)</td><td>440(PQ.05)</td><td>438(PQ.03)</td><td>317(PCC.00)</td><td>318(PCC.01)</td></tr><tr><td>ORIN NX</td><td>453(PQ.05)</td><td>446(PP.06)</td><td>328(PCC.00)</td><td>329(PCC.01)</td></tr><tr><td>ORIN NANO</td><td>453(PQ.05)</td><td>446(PP.06)</td><td>328(PCC.00)</td><td>329(PCC.01)</td></tr></table>		GPIO01	GPIO02	GPIO03	GPIO04	Xavier NX(<=L4T32.*)	421	419	264	265	Xavier NX(>L4T 32.*)	440(PQ.05)	438(PQ.03)	317(PCC.00)	318(PCC.01)	ORIN NX	453(PQ.05)	446(PP.06)	328(PCC.00)	329(PCC.01)	ORIN NANO	453(PQ.05)	446(PP.06)	328(PCC.00)	329(PCC.01)							
	GPIO01	GPIO02	GPIO03	GPIO04																												
Xavier NX(<=L4T32.*)	421	419	264	265																												
Xavier NX(>L4T 32.*)	440(PQ.05)	438(PQ.03)	317(PCC.00)	318(PCC.01)																												
ORIN NX	453(PQ.05)	446(PP.06)	328(PCC.00)	329(PCC.01)																												
ORIN NANO	453(PQ.05)	446(PP.06)	328(PCC.00)	329(PCC.01)																												
Description: Take the Xavier NX module, GPIO02, as an example, if the system version is L4T32.*, run this command: \$ echo 419 > /sys/class/gpio/export After GPIO is enabled, the corresponding file name is generated: gpio419; Then system version is later then L4T 32.*, run this command: \$ echo 438 > /sys/class/gpio/export After GPIO is enabled, the corresponding file name is generated: PQ.03.																																
Pin 1 position: right picture identification. No welding by default																																

6 Ordering Information

Order Type	Function
Y-C17	NVIDIA® Jetson™ ORIN NX/ORIN NANO/Xavier NX series module is equipped with miniaturized carrier board.

E-commerce Platform

Taobao Store Address: <https://shop333807435.taobao.com/>

Jingdong Store Address: <https://mall.jd.com/index-11467104.html?from=pc>

Ali International Station Address: <https://plink-ai.en.alibaba.com/>

7 Recovery Mode

Jetson core module can work in normal mode and Recovery mode. In Recovery mode, it can perform file system update, kernel update, Bootloader/UEFI update, BCT update and other operations. Y-C17 needs to be matched with the company's supporting signal separation board before it can enter the recovery mode and perform the above operations.

To enter the Recovery mode, perform the following steps :

- Power off the system;
- Connect the signal separation board A face up to the Type-C port (J2) of Y-C17;
- Use the Micro-USB cable to connect the Micro-USB port of the signal separation board with the USB port of the Jetson development host.
- Hold down the Recovery button on the signal separation board, **and then supply power to the system.** After power supply, keep the Recovery button pressed for more than 3 seconds, and then release the Recovery button.
- The system enters Recovery mode, at which time subsequent operations can be performed.

8 Method of Application

- Make sure all external system voltages are off.
- Install the Jetson core module onto the J1 high-speed connector. Ensure that the connectors are aligned with even force. After the module is installed in place, install the core module fixing screws.
- Install necessary external cables. (such as: the display line connected to the HDMI display, the power input line for the system power supply, the USB cable connecting the keyboard and mouse...)
- Connect the power cable to the power supply.(Make sure that the heat dissipation device on the core module is installed before power-on)
- For a system without a protective cover, do not move the hardware system after the system is powered on. Do not touch the circuit board or any electronic components on the circuit board with your body.

9 GPIO Test

Y-C17 with Jetson module comes standard with 4 GPIOs. Programmable output voltage 3.3V, please note that the input voltage does not exceed 3.3V.

Take L4T35.3.1, GPIO02 as an example when equipped with ORIN NX module:

The content after the '#' in the following command is a comment and does not need to be added when executing the command.

- `sudo su`
- `echo 446 > /sys/class/gpio/export #Enabel GPIO (Or initializeGPIO)`
- `echo out > /sys/class/gpio/PP.06/direction`

`# Set the GPIO input and output directions to out or in.`

- `echo 1 > /sys/class/gpio/PP.06/value`
`# Set the GPIO output high/low level to 1 for high and 0 for low.`

The preceding absolute path name is based on the actual path name generated after GPIO is enabled.

When set to the input state, you can only read values. When set to the output state, you can read and write values.

- `cat /sys/class/gpio/PP.06/value #Get GPIO value.`

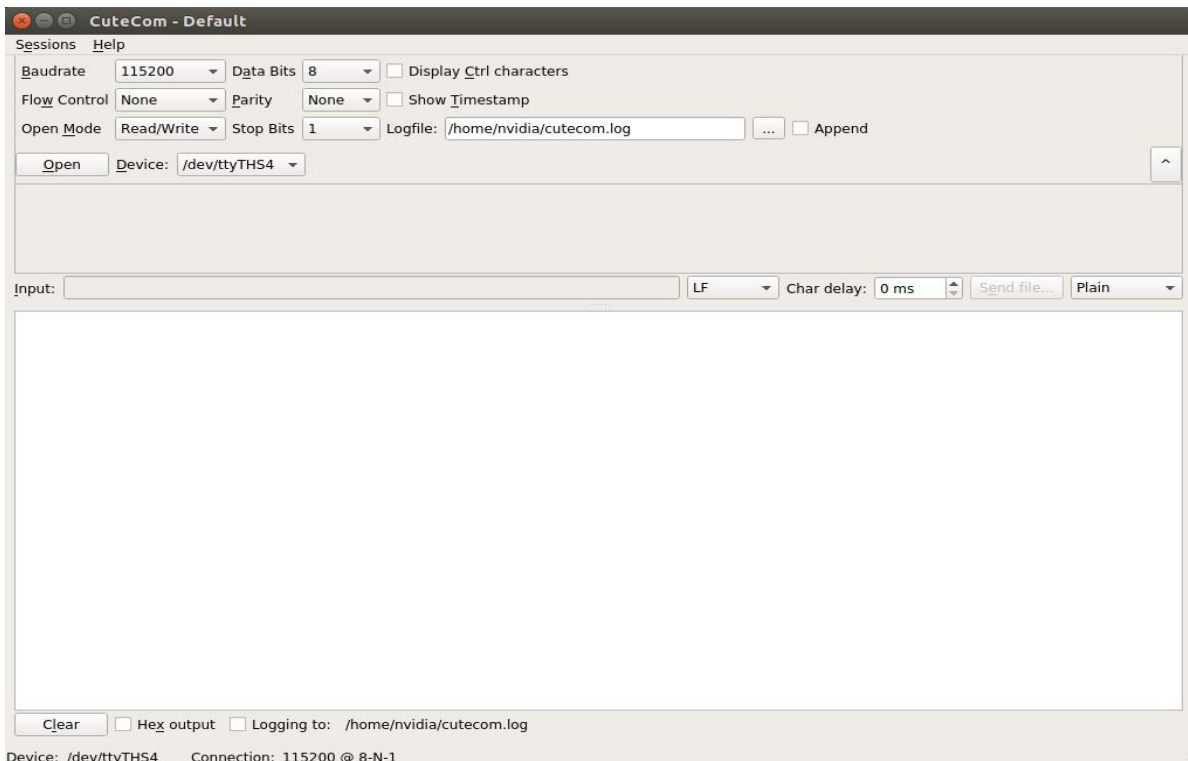
The output state can be measured using a multimeter to measure the voltage between the specific lead heel GND.

10 Serial Port Test

Y-C17 is equipped with two 3.3V TTL serial ports as standard when it is paired with Jetson module, which can be used for self-collecting test of a single serial port and interconnection test of two serial ports. The command is as follows:

- `sudo apt-get install cutecom` #Install the serial port test tool
- `sudo cutecom` # For a single-serial port test, you only need to open one cutecom interface on each terminal. For a two-serial port connection test, use two terminals and open two cutecom interfaces.
- When testing a single serial port, connect the RX of a single serial port to the TX. When the two serial ports are connected, the RX of UART1 is connected to the TX of UART2, and the TX of UART1 is connected to the RX of UART2.

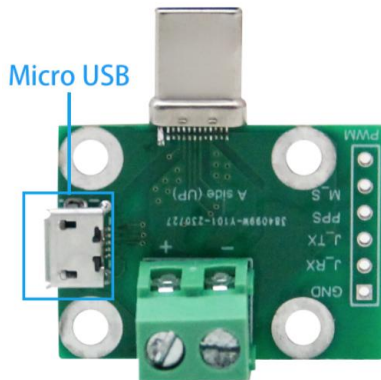
The interface of the serial port test tool cutecom is as follows:



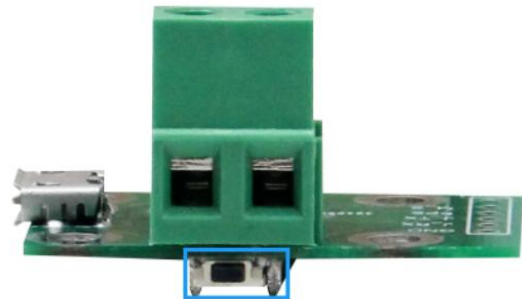
11 Special Instructions

- Initial system username: **nvidia** , password: **nvidia**, no password su. If root permissions are required, use sudo to grant permissions, or use sudo su to access the root user.
- The pre-installed system is pure by default and does not contain Jetpack software. You can use the following command to install the software. Do not replace or modify the default software source before installation:
 - `sudo apt-get update`
 - `sudo apt-get install nvidia-jetpack`
- It can also be installed over the network using SDKmanager software.
- For more information please refer to :Jetson wiki (plink-ai.com)

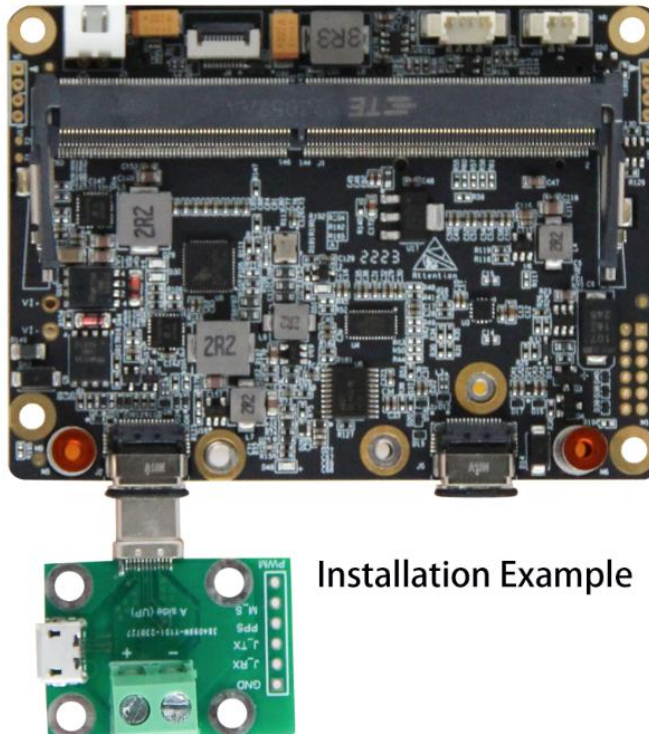
12 Signal Separation Board



A Side



Recovery Button



Installation Example